RESUME

S.Maragatharaj,
203/110A, Ariyagoundampatti,
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OBJECTIVE

To embark a career in creative and challenging environments, which will enable me to deploy my professional, education and functional talents in the best possible way to reach goals of the institution, myself and the society as whole.

EDUCATIONAL DETAILS

1) ***Course:*** Ph.D.
Faculty/ Institution: Information and Communication Engineering.
University: Anna University, Chennai, India.
Status: Registered in 2016

2) ***Course:*** **Master of Engineering** (VLSI Design)
Faculty/ Institution: Dept. of ECE, Anna University of Technology, Coimbatore.
University: Anna University of Technology, Coimbatore, India.
CGPA: 8.11
Year of Completion: 2011

3) ***Course:*** **Bachelor of Engineering** (Electronics and Communication Engineering)
Faculty/ Institution: Annai Mathammal Saheela Engineering College, Salem.
University: Anna University, Chennai, India.
Percentage: 68%
Year of Completion: 2008

4) ***Standard:*** **HSC**
Institution: Ideal Hr. Sec. School, Anthiyur, Erode District.
Percentage: 82.5%
Year of Completion: 2004

5) ***Standard:*** **SSLC**
Institution: Sri Vidhya Mandir Matric. Hr. Sec. School, Salem District.
Percentage: 76.5%
Year of Completion: 2002

SERVICE DETAILS

S.No.	Name of the Institution	From	To	Duration
1	Knowledge Institute of Technology, Salem	June 2012	May 2018	6 Years
2	The Kavery Engineering College	June 2011	May 2012	11 Months

AREA OF INTEREST

1) Microprocessors and Microcontrollers
2) VLSI Design
3) Low Power VLSI
4) Advanced Microprocessors
5) Green Technology & Sustainability

TECHNICAL PUBLICATIONS

International Journals:

1. "Modified Routing Protocol for Defending Against Attacks in MANET", International Journal for Advanced Research in Computer Science and Software Engineering, Vol.2, Issue 1, 2012, pp.12-16.ISSN:2277128X (Impact Factor: 2.5)
2. "Papr Reduction Based on Clipping and Scaling Approach in Multiplexing Systems Using Mat lab", International Journal of Communications and Engineering, Vol.5,Issue 2, March 2012.ISSN: 09880382E
3. "A Novel Method Of Ambulance Service Time Reduction Using Zigbee", International Journal of Advance Research in Science and Engineering, Vo2, April 2013
   ISSN: 2319 8354
4. "Analysis of Different Bit Carry Look Ahead Adder Using verilog Code", International Journal of Electronics and Communication & Technology, Vol. 4, August 2013. ISSN: 2230 7109
5. "Simulation of QCA Based Binary to BCD Converter in Xilinx using HDLQ", imanager's Journal of Electronics Engineering, Vol. 1, August 2013.ISSN:2229 7286
6. "QCA Based Low Power Parallel Binary Adder Subtractor using Reversible Logic Gates", imanager's Journal of Electronics Engineering", Vol. 1, February 2014. ISSN:2229 7286

7. "Design of finite impulse response filter using distributed arithmetic of look up table", International journal of innovative research in science, engineering and technology,Vol.4 special issue 6, may 2015, ISSN: 2319 8753(Impact Factor: 6.2)
8. "Raspberry Pi based interactive home automation system through Internet of things", International journal for research in applied science & engineering technology, Vol.3, Issue 11, March 2015, pp 809-814, ISSN: 2321 9653 (Copernicus Index: 13.98)
9. "FPGA Implementation of Area Efficient Finite Field Redundant Multipliers", International Journal for Scientific Research & Development, Vol. 5, Issue 03, 2017,ISSN(online):2321-0613

Conferences:

1. "Performance Analysis of Power Gating designs in Low Power VLSI Circuits" proc. of international conference on signal processing, communication, computing and networking technologies, February 2011
2. "Design of Energy and Area Efficient Low Power Carry Select Adder" proc. of International Conference on Advances in Engineering and Technology, May 2011
3. "Nano scale Based Area, Delay and Power comparison of Adder topologies"
4. Presented a paper on "Enhanced Non-Traditional Learning Environment for Communication Engineers Using Free Open Source Software Tools", proc. of International Conference on Technology for Education, December 2013
5. "Effective Binary to BCD Converter using Quantum Dot Cellular Automata", proc. of International Conference on Devices Circuits & Systems, January 2014
6. "FPGA Implementation of FIR filter using Effective Distributed Arithmetic Algorithm", proc. of International Conference on Developments in Engineering Research, December 2014
7. "Raspberry Pi based Interactive Home Automation System through Internet of Things", proc. of International Conference on Recent Innovations in Engineering & Technology, March 2015
8. Safety Helmet for Coal Miners", proc. Of National Conference on Communication Technology Interventions for Rural and Social Development, March 2017

WORKSHOP PARTICIPATION

1. Participated in one day workshop on “Mentor Graphics based VLSI design flow” conducted by Anna University of Technology, Coimbatore
2. Participated in six day Faculty Development Program on “VLSI Design” conducted by Jansons Institute of Technology, Coimbatore
3. Participated in one day workshop on “Renesas Microcontrollers” conducted by Government College of Engineering, Salem
4. Participated in one day workshop on “Ultra Low Power Mixed Signal Processor-MSP 430” conducted by Tenet Technologies, Bengaluru
5. Participated in one day workshop on “Teacherpreneurship” conducted by Confederation of Indian Industries, Salem
6. Participated in three day workshop on “Mission 10X” conducted by Wipro
7. Participated in ten day workshop on “Analog Electronics” conducted by IIT-Kharagpur
8. Participated in fifteen day workshop on “Advances in Medical Imaging Using Computational Intelligence”
9. Participated in two day workshop on “Awareness and Training for Faculty about New Outcome Based Accreditation(OBA) process of NBA”, conducted by Jayam College of Engineering and Technology, Dharmapuri
10. Co-Ordinated a two day national seminar on ”Real Time Embedded Solutions for Domestic Environment”
11. Participated in ten day workshop on “Signals and systems” conducted by IIT-Mumbai
12. Participated in ten day workshop on “Control Systems” conducted by IIT-Kharagpur
13. Participated in two week workshop on “Environmental Engineering” conducted by IIT-Mumbai
14. Participated in two week STTP on “CMOS, Mixed Signal and Radio Frequency VLSI Design”, conducted by IIT-Kharagpur

MEMBERSHIP IN PROFESSIONAL SOCIETIES

1. Life time member of Indian Society for Technical Education (ISTE)
   Member ID: LM107419.
2. Associate Member of Universal Association of Computer and Electronics Engineers (UACEE) Member ID: AM10100057191.
3. Member of International Society for Research and Development (ISRD)
   Member ID: M4150901661.

COURSES UNDERTAKEN & CONTEST

1. Completed MOOC course on "Education Technology for Engineering Teachers" conducted by IIT-Bombayx (13th March 2016)
2. Selected for the final round of KALPANA CONTEST 2016, conducted by IIT-Mumbai and Tata Centre for Technology & Design. (25th May 2016)
3. Completed MOOC course on "Academic Integrity" conducted by University of Auckland, New Zealand (03rd October 2016)
4. Completed MOOC course on "Hardware modelling using Verilog" conducted by Swayam platform.
5. Selected for Quarterfinals of India Innovate Challenge Design Contest-2017, conducted by Texas Instruments & DST.

PERSONAL DETAILS

Name:	S. MARAGATHARAJ
Father Name:	P.SELVARAJ
Date of Birth:	05-11-1986
Sex:	Male
Marital Status:	Married
Nationality:	Indian
Languages Known:	English, Tamil

DECLARATION

I hereby declare that the information furnished above is true to the best of my knowledge.

Date:

Place: Salem

(S.MARAGATHARAJ)